Claims

Claim 1. (Currently Amended) A method of decomposing timing jitter on a signal under test (SUT) comprising an arbitrary serial data stream, said method comprising:

forming a group of measurements, where each measurement ~~comprises~~ includes a timing jitter value and an associated bit pattern representing ~~the~~ bits falling within an analysis window of a chosen length, said analysis window being successively located at a plurality of positions within the SUT; and

performing a statistical analysis on said group of measurements to calculate ~~the~~ a mean value of ~~the~~ inter-symbol interference (ISI) associated with each bit pattern.

Claim 2. (Currently Amended) The method of claim 1, wherein said ISI ~~jitter~~ is determined for a specified edge polarity only.

Claim 3. (Currently Amended) The method of claim 1, further comprising separating random and periodic jitter from said timing jitter.

Claim 4. (Original) The method of claim 1, further comprising estimating duty cycle distortion (DCD) from said timing jitter.

Claim 5. (Currently Amended) The method of claim 4, further comprising removing said DCD from ~~a record~~ said timing jitter.

Claim 10. (Currently Amended) The test and measurement device of claim 9, wherein said processing module is further for determining said ISI ~~jitter~~ for a specified edge polarity only.

Claim 11. (Currently Amended) The test and measurement device of claim 9, wherein said processing module is further for separating random and periodic jitter from said timing jitter.

Claim 12. (Original) The test and measurement device of claim 9, wherein said processing module is further for estimating duty cycle distortion (DCD). from said timing jitter

Claim 13. (Currently Amended) The test and measurement device of claim ~~9~~ 12, wherein said processing module is further for removing said DCD from ~~a record~~ said timing jitter.

Claim 14. (Currently Amended) The test and measurement device of claim 9, wherein said processing module is further for removing said ISI from ~~a record~~ said timing jitter.

Claim 15. (Currently Amended) A computer-readable media for storing software instructions which when executed by a processor perform the steps of:

decomposing timing jitter on a signal under test (SUT), the SUT being ~~comprising~~ an arbitrary serial data stream, by

forming a group of measurements, where each measurement ~~comprises~~ includes a timing jitter value and an associated bit pattern representing ~~the~~ bits falling within an analysis window of a chosen length, said analysis window being successively located at a plurality of positions within the ~~SUT~~ arbitrary serial data stream; and

performing a statistical analysis on said group of measurements to calculate ~~the~~ a mean value of ~~the~~ inter-symbol interference (ISI) associated with each bit pattern.

Claim 16. (Currently Amended) The computer-readable media of claim 15, wherein said ISI ~~jitter~~ is determined for a specified edge polarity only.

Claim 17. (Currently Amended) The computer-readable media of claim 15, further comprising instructions for separating random and periodic jitter from said timing jitter.

Claim 18. (Original) The computer-readable media of claim 15, further comprising instructions for estimating duty cycle distortion (DCD). from said timing jitter

Claim 19. (Currently Amended) The computer-readable media of claim ~~15~~ 18, further comprising instructions for removing said DCD from ~~a record~~ said timing jitter.

Claim 20. (Currently Amended) The computer-readable media of claim 15, further comprising instructions for removing said ISI from ~~a record~~ said timing jitter.